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AN EFFICIENT DESIGN OF 1 BIT ARITHMETIC LOGIC UNIT IN QUANTUM DOT CELLULAR AUTOMATA

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ABSTRACT

Quantum cellular automata (QCA) is an attractive emerging technology that takes advantage of quantum effects, which become increasingly apparent at the scale of a few nanometers. Previous work has shown that QCA has several novel features not available with conventional FET-based circuits. We describe the design of 1-bit Arithmetic Logic Unit based on combinational circuits which reduces the required hard-ware complexity and allows for reasonable simulation times. Our aim is to provide evidence that QCA has potential applications in future computers provided that the underlying technology is made feasible. The 1-bit Arithmetic logic unit (ALU) consist arithmetic unit, logical unit and full adder are major blocks of ALU. The design of ALU is successfully implemented using QCADesigner tool and also verified the simulation result of 1-bit ALU.

Keywords- Arithmetic Logic Unit, Nanotechnology, QCA

INTRODUCTION

Quantum Cellular Automata (QCA) refers to quantum computation, which have been devised in analogy conventional models of cellular automata introduced by von Neumann. The QCA also refer to quantum dot cellular automata, which proposed the physical implementation of "classical" cellular automata exploiting quantum mechanical phenomena. Quantum Cellular Automata has attracted a lot of attention as a result of its extremely small feature size (at the molecular or even atomic scale) and its ultra low power consumption, making it one candidate for replacing CMOS technology. In QCA, a quantum cell normally consists of four quantum dots at corner of a square, with two excess electrons that are free to tunnel between the dots but which cannot leave the cell. As per coulomb repulsion, these two electrons tend to occupy diagonally opposite dots. In a second type of QCA cell, the dots are located at the middle of the side of the cell, instead of the corners. In either cell type, there are just two configurations with energetically equivalent polarization designated as +1 and -1. This means that quantum cells can be employed as binary system to represent logical true and false (or digital 1 and 0). Moreover, multiple quantum cells can be arranged in various linear formations to produce logic gates, which can in turn be used to build devises foe computation. The basic logic elements in QCA logic are the majority gate and the inverter (or NOT gate). An arithmetic and logic unit (ALU) is a digital circuit that performs the arithmetic and logical operations. The ALU is a basic building block of the central processing unit of a computer, and the microprocessors contain one for maintaining timers. The processor found inside the CPUs and graphics processing units (GPUs) suit very powerful and very complex LAUs; a single component may contain a number of ALUs. The ALU concept proposes by Mathematician John von Neumann in 1945. He wrote a report on foundation for a new computer called the EDVAC. Research into ALUs remains an important part of computer science, falling under arithmetic and logic structure in the ACM Computing Classification System

QCA REVIEW

A. Background

The basic building block of QCA devices named cell is presented in Fig. 1(a). QCA cell consists of four quantum dots in a square array coupled by tunnel barriers, two electrons are injected into the cell. Due to Coulombic repulsion, the two electrons reside in opposite corners representing two polarizations. Some basic elements for QCA logic implementation are the wire, inverter, and majority voters as shown in Figure No. 1.

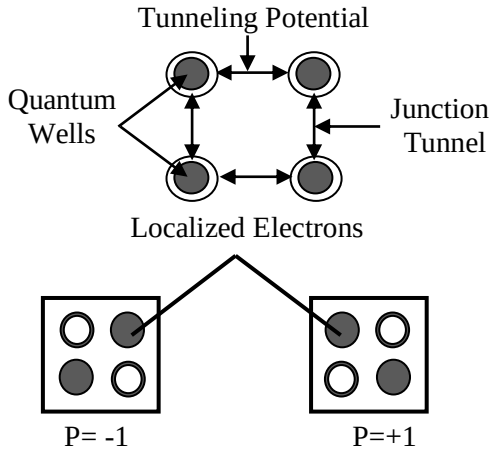


Figure No. 1(a): QCA cell and its Polarization

QCA wire is formed by an array of QCA cells shown in Figure No. 1(b), which provides a medium for data propagation based on Coulomb interactions.

Figure No. 1(b): QCA Wire

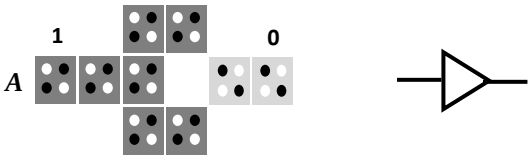


Figure No. 1(c): QCA inverter

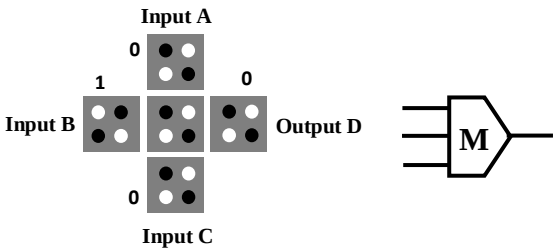


Figure No. 1(d): QCA Majority Voter

The polarization of the output QCA cell 'out' or 'output' is the opposite of the polarization of input QCA cell 'in' or 'input'. QCA majority voter (MV) and its logic symbol are shown in Figure No. 3(a), MV, is equivalent to a logic function F(A,B,C)=AB+AC+BC and can be implemented by five QCA cells arranged in a cross. Cells A, B, and C are input cells, and cell D is the output cell that is polarized according to the polarization of the majority of the input cells. For example, since two (out of three) input QCA cells are polarized to -1. The output cell is also polarized to be -1 (see Figure No. 3(b)). Logical AND and OR functions can be implemented from majority voter by presetting one input immutably to binary values 0 and 1, respectively [1-5],[8].

B. QCA Clocking

A QCA cell has four clock phases; they are Switch, Hold, Release and Relax [6, 7]. Figure No. 2 shows four phases of the QCA clock operation process. During the switch phase, QCA cells begin un-polarized and their inter dots potential barriers are low. The barriers are then raised during this phase, and the QCA cells become polarized according to the state of their driver (i.e. their input cell). It is in this clock phase that the actual computation (or switching) occurs. By the end of this clock phase, barriers are high enough to suppress any electron tunneling and cell states are fixed. During the hold phase, barriers are held high so the outputs of the sub array can be used as inputs to the next stage. In the release phase, barriers are lowered and cells are allowed to relax to an un-polarized state. Finally, during the fourth clock phase, the relax phase, cell barriers remain lowered and cells remain in an

un-polarized state [6, 7]. In the meantime, the large scale QCA circuit is partitioned into four clock zones; Figure No. 2 shows each clock zone signal and demonstrates the pipeline mechanism. All cells in a certain zone are controlled by the same QCA clock signal. Cells in each zone perform a specific calculation; the state of a zone is then fixed so that it can serve as input signals to the next zone. Information transfers in a pipelined fashion.

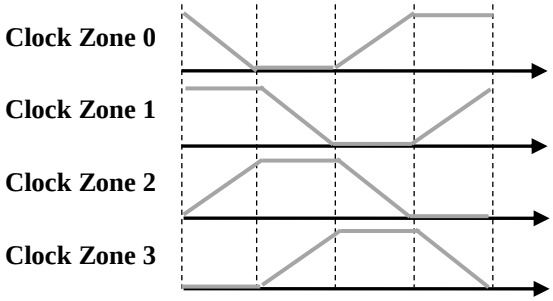
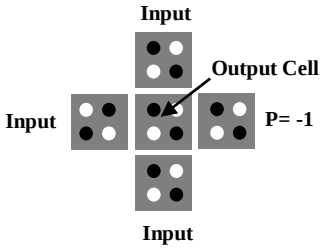


Figure No. 2: Clocking Zones

C. Three-bit AND & OR using Majority Voter Gate



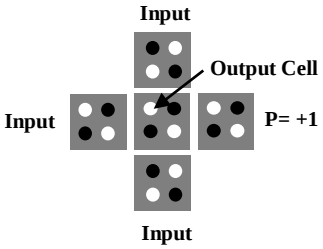


Figure No. 3 (a) 3-bit AND **Figure No. 3 (b) 3-bit OR**

ARCHITECTURE OF ARITHMETIC LOGIC UNIT

An Arithmetic Logic Unit (ALU) is a multi-operation, combinational-logic digital function. It can perform a set of basic arithmetic operations and a set of logic operation. The ALU has a number of selection lines to select a particular operation in the unit. The Arithmetic Logic Unit consists three basic units; arithmetic unit, logical unit and full adder circuit. In addition to these operations it also takes AND of two numbers and OR of two numbers. M and S are the select signals that decide which operation are performed. M is a select line to select operations either arithmetic or logical. The function table for the four operations performed by the ALU is shown in Table No. 1.

S. No.	Select		Operation	Functions
	S1	S0		
Logical Operations				
1	0	0	AND	A&B
2	0	1	OR	A|B
Arithmetic Operations				
3	1	0	Addition	A+B
4	1	1	Subtraction	A+B'+1

Table No. 1: Function Table of Arithmetic Logic Unit

A. Arithmetic Unit

The Arithmetic Unit modifies the second operand and passes it to the Full Adder to perform the arithmetic. Arithmetic is the oldest and most elementary branch of mathematics, used by almost everyone, for tasks ranging from simple day-to-day counting to advanced science and business calculations. It involves the study of quantity, especially as the result of operations that combine numbers.

$$Y = S_1\bar{S_0}B + S_1S_0\bar{B}$$

$$C_0 = S_1S_0$$

S_1	S_0	A	B	Y
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

Table No. 2: Truth table of Arithmetic Unit

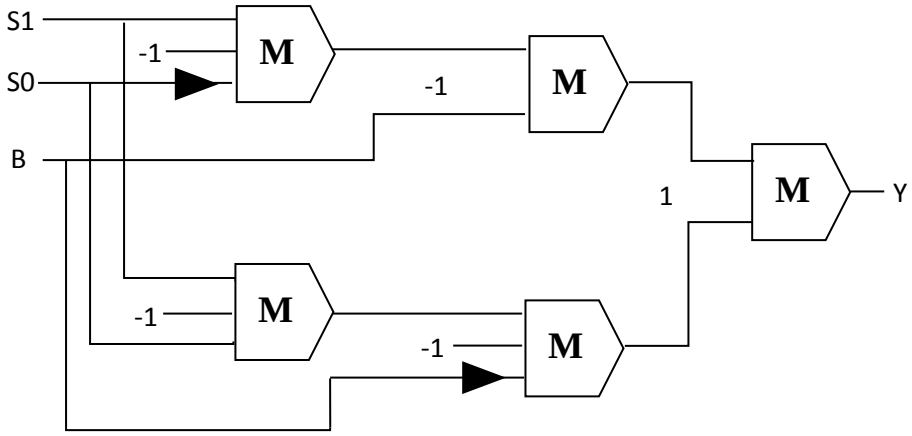


Figure No. 4: Schematic diagram of Arithmetic Unit

B. Logical Unit

The logic operations are performed in the logic Unit. The Full adders are used simply as connections for the outputs. In logic and mathematics, a two-place logical operator and, also known as logical conjunction, results in true if both of its operands are true, otherwise the value of *false*.

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S_1	S_0	A	B	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1

Table No. 3: Truth Table of Logical Unit

$$X = \bar{S}_1 S_0 B + AB + S_1 A + S_0 A$$

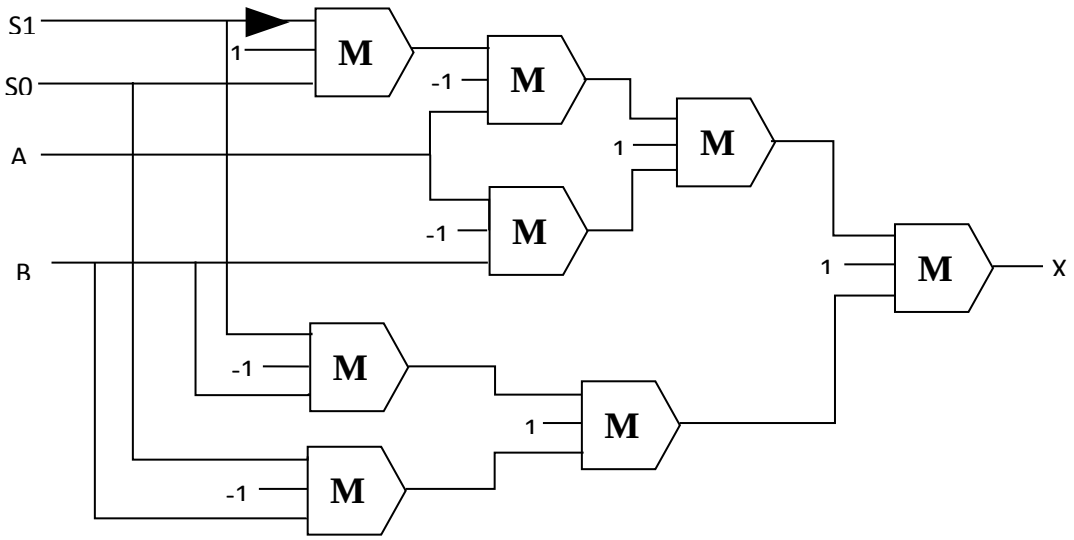

Figure No. 5: Simplified schematic diagram of logical Unit

IMPLEMENTATION OF 1 BIT ALU IN QCA

Implementation of one bit ALU in QCA is verified using QCA Designer tool. The proposed design is shown in Figure No. 6.

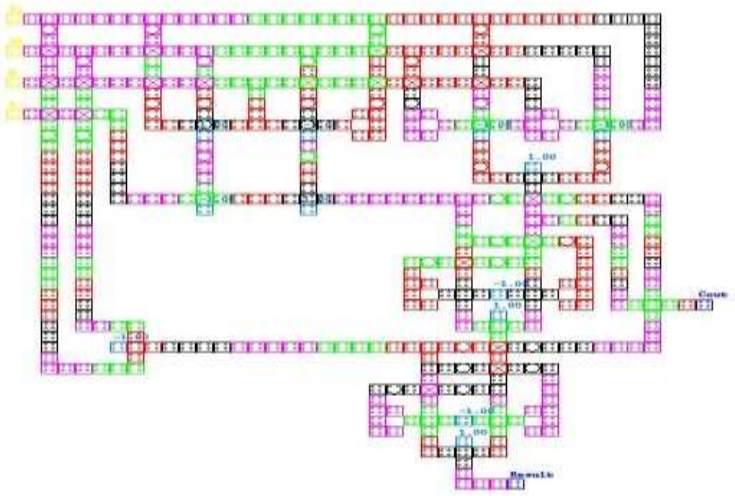

Figure No. 6: Implementation of 1 bit ALU in QCA

SIMULATION RESULTS AND DISCUSSION

All the designs were verified using QCADesigner tool ver. 2.0.3. In the bi-stable approximation, we used the following parameters: cell size=18 nm, number of samples=12800, convergence tolerance=0.001000, radius of effect=65.00 nm, relative permittivity=12.900000, clock high=9.800000e-022, clock low=3.800000e-023, clock amplitude factor=2.000000, layer separation=11.500000, maximum iteration per sample=100. All of these parameters which used are default parameters in QCADesigner tool. In our QCA layouts, we have the goal of workable designs with compact layout. The simulation Results of one bit ALU is shown in Figure No. 7.

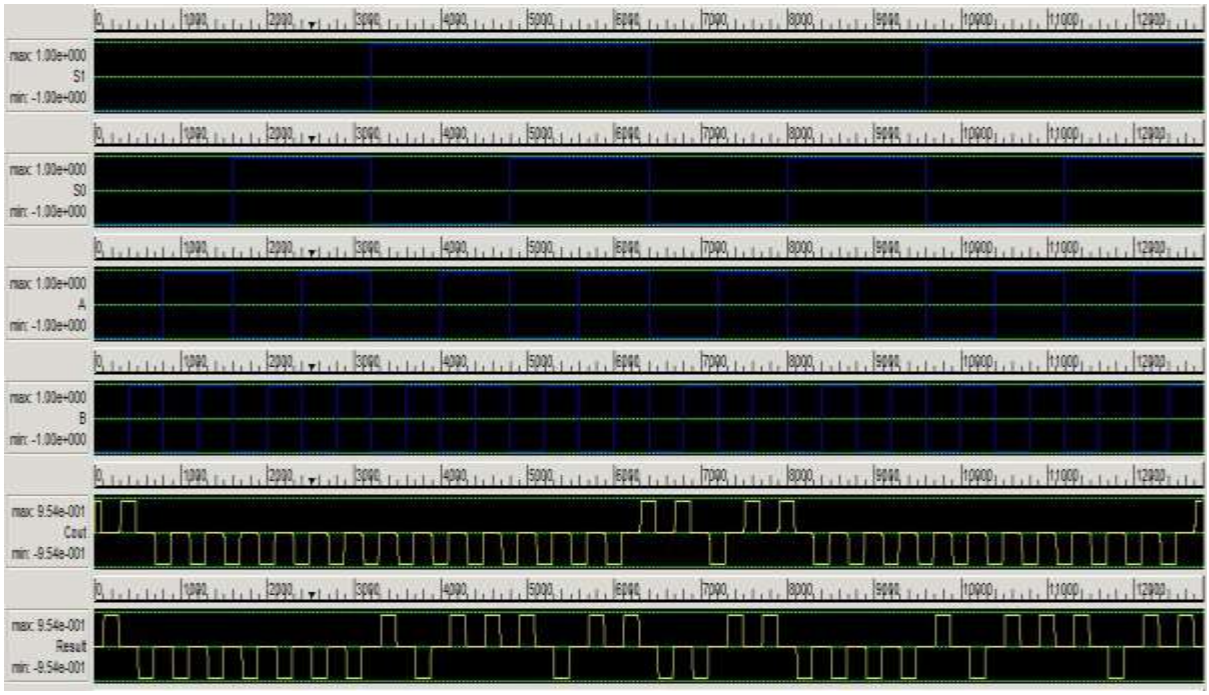

Figure No. 7: Simulation result of 1 bit ALU

CONCLUSION

This paper proposes one bit ALU (Arithmetic Logic Unit) in QCA which uses arithmetic and Logical Extender and Full adder. The proposed work shows that the Functions of ALU design in QCA is same as traditional ALU designed in CMOS technology. By using QCA we have reduces complexity, size, power consumption, delay & cost and Improve the performance of ALU is much beneficial.

In future, we will design 2-bit, 4-bit & 8-bit ALU in QCA. We will also design 1-bit ALU (Arithmetic Logic Unit) using Reversible logic gates in QCA.

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